3.0 Introduction

This chapter concerns about the control logic and register part of the whole circuit. It provides detail about this part with the implementation process. It also gives information about how it works.

3.1 The implementation process:

This was the main part of the successive approximation A/D converter since it produces the parallel digital output, regulates the circuit operations, tells the circuit when to start and when to stop, and it decides how long the conversion time is. Figure 1.3 in chapter 1 shows that the circuit mainly consists of:

- An 8-bit shift register.
- AND gates.
- JK flip-flops.

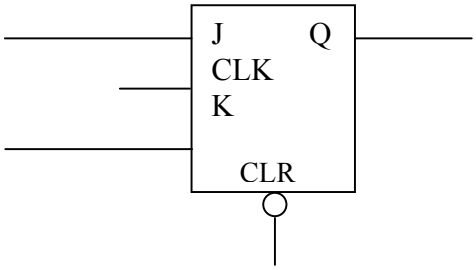
Also there are some other supporting components such inverters and delays.

This circuit could be designed in many ways using different components, but at the same time this design was subjected only to the components, which are available in the design manger software.

The main idea of this design was to implement a circuit which performs the same behavior of the successive approximation that is dependent on the comparator output which tells the circuit to either leave a bit high (1) or low (0) to produce the correct binary output.

Such behavior needed flip flops with more than one input one for zero (low state) while the second one for setting the flip flop at one (high state) this can be easily done using SR flip flops or JK flip flops but only JK was available in the software, so it is been used in the design process. Figure 3.0 in the next page shows the JK flip flop construction and it is behavior:

OUTPUTS		INPUTS	
Q	**Q+**	**J**	**K**
0	0	0	X
0	1	1	X
1	0	0	1
1	1	1	0



Q = present state, Q+ = next state

CLK = clock input.

CLR = clear input (active low)

When J = 1 flip flop is set to 1(Q = 1)

When K=1 flip flop is reset to 0 (Q = 0)

Figure 3.0 The block diagram and the excitation table of JK/FF.

The second problem in designing the control logic was how to shift from one bit to the next bit in a regular way. This was achieved by using an 8-bit shift register for the eight bit digital output. Another problem arose here with the positive edge trigger flip-flops in the register and the negative edge trigger JK flip-flops. That is shown in figure 3.1 in the next page.

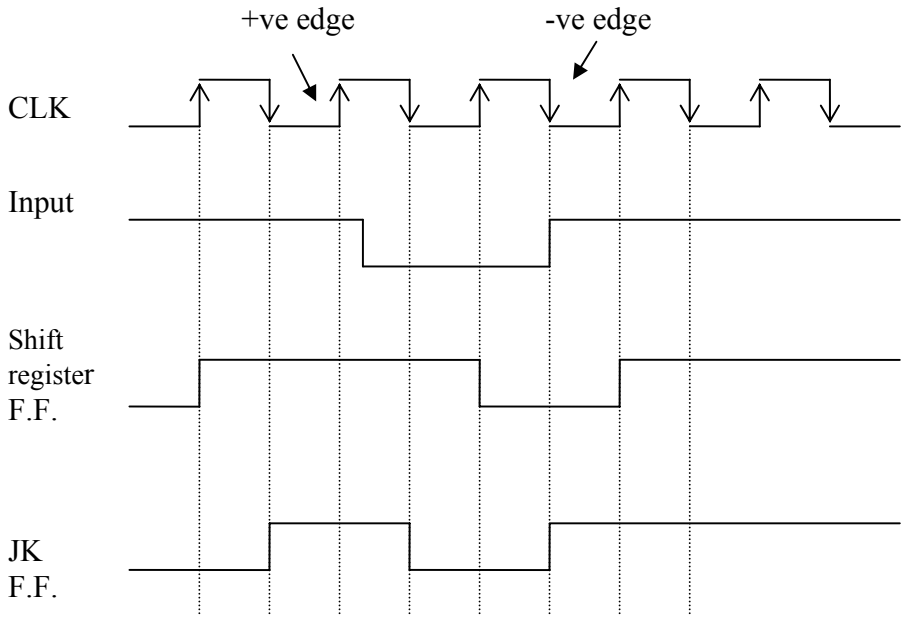


figure 3.1 the positive and negative triggers

This problem was solved through placing an inverter before the register CLK input to synchronize all flip-flops with the register.

The AND gates were connected in such a way that the K inputs would be high or low depending on the comparator output during each clock cycle. The comparator input is an active low input. The control logic circuit is shown in the next page figure 3.2

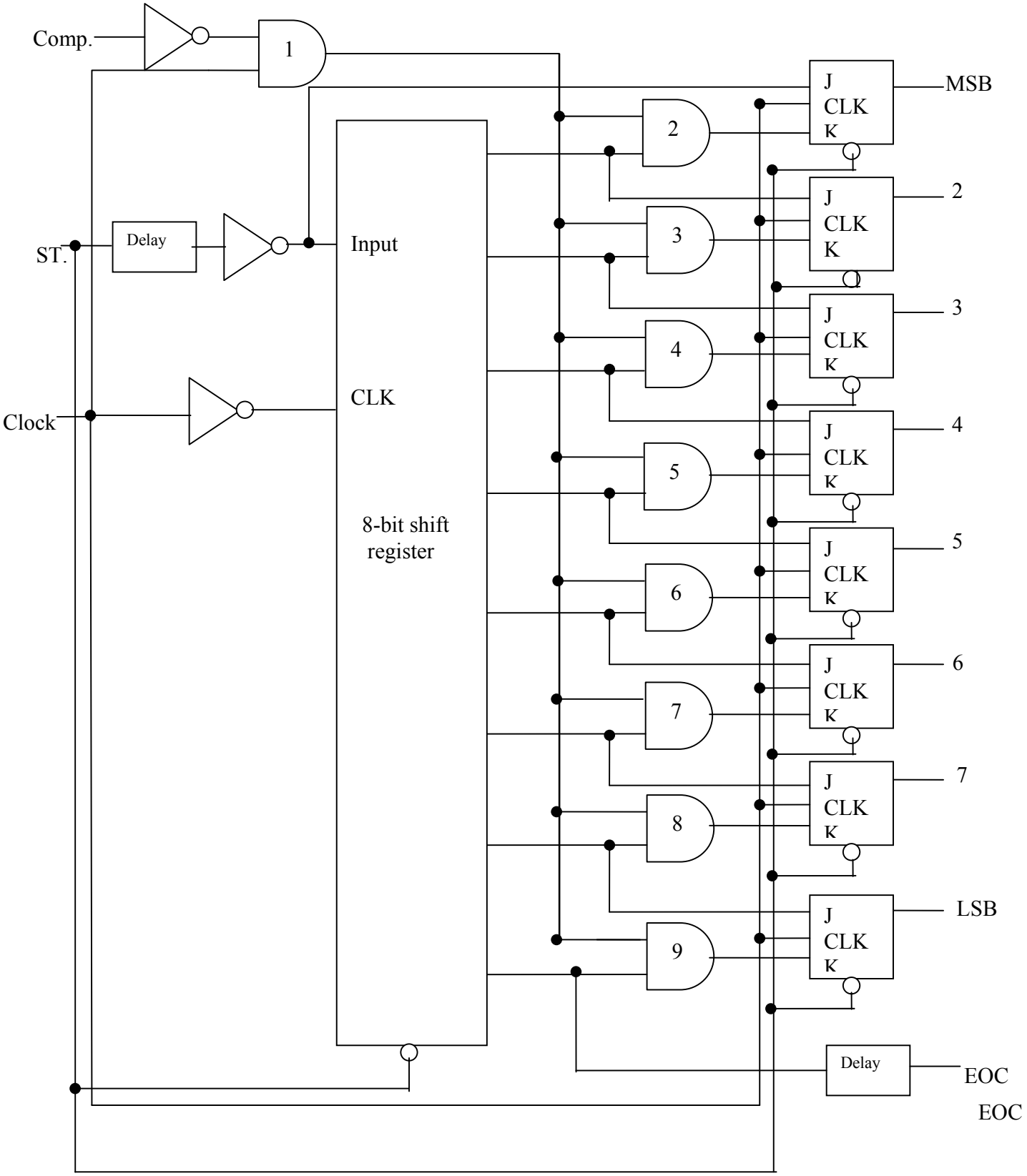


Figure 3.2: The control Logic circuitry.

3.2 How does it work?

In the first clock cycle the start pulse comes into the logic circuit. It clears all the bits forcing them to be at low logic level (0).

Then it begins checking each bit starting from MSB by forcing each of them to be high but before it moves from one bit to the next, it checks the comparator output. If the comparator output is high then the bit will stay as it is otherwise the bit will be reset back to zero.

The Comparator output

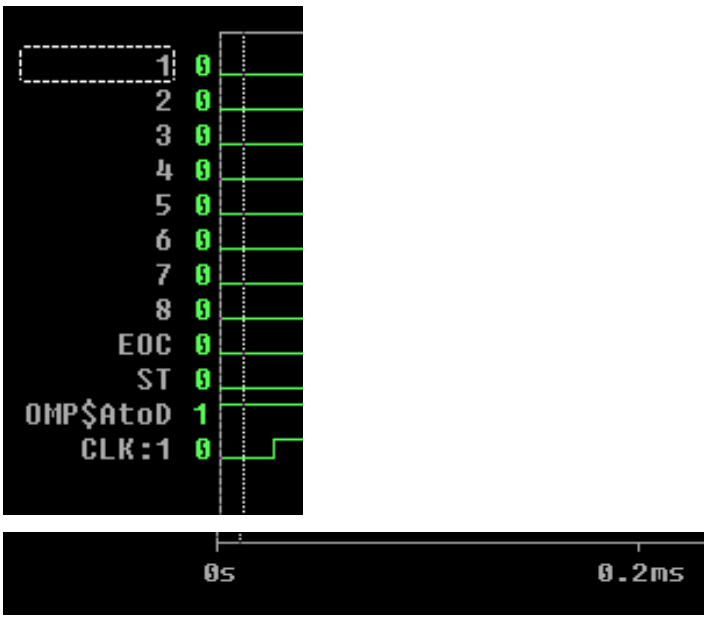


Figure 3.3: The output of the control logic circuit at the start pulse. This figure was taken from Design Manager Software where 1 to 8 bits are the MSB to LSB bits, (ST) is the start pulse which was at Zero level since all clear inputs are active Low.

The same START pulse is delayed enough before going into and setting one in the first flip flops of the shift register as well as the first JK flip flop which is the MSB as shown in figure 3.4in the next page.

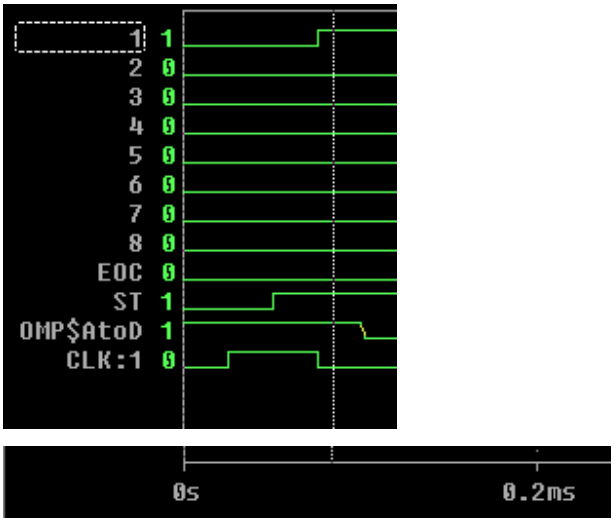


Figure 3.4: After the start pulse the bit 1 (MSB) becomes directly one.

During the next clock pulse as the one in the first bit of the shift register is shifted to the next bit, AND gate (2) either removes or leaves the one in the MSB depending on the comparator output that appears at the output of gate (1) and the Next MSB is set to ONE state which can also be left as one or reset to zero depending on the comparator output as shown in figure 3.5 below.

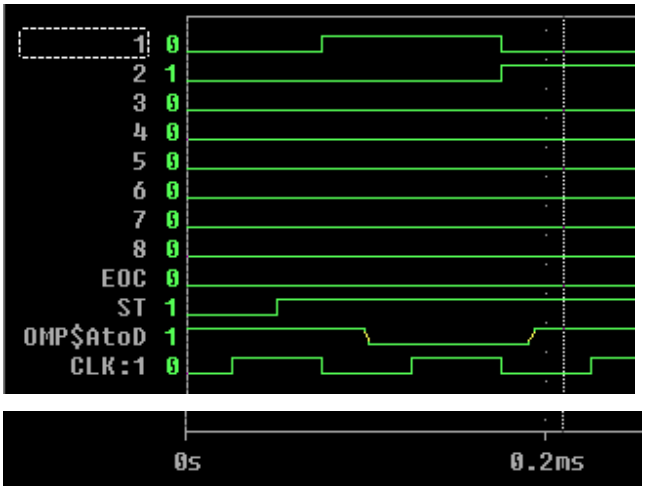


Figure 3.5: After the second CLK pulse the MSB went to Zero level as the comparator output was Zero. At the vertical line after 0.2ms the next bit is one.

This process is repeated on all bits until reaching to the LSB. And directly the EOC (End Of Conversion) pulse is sent to informing the end of conversion process.

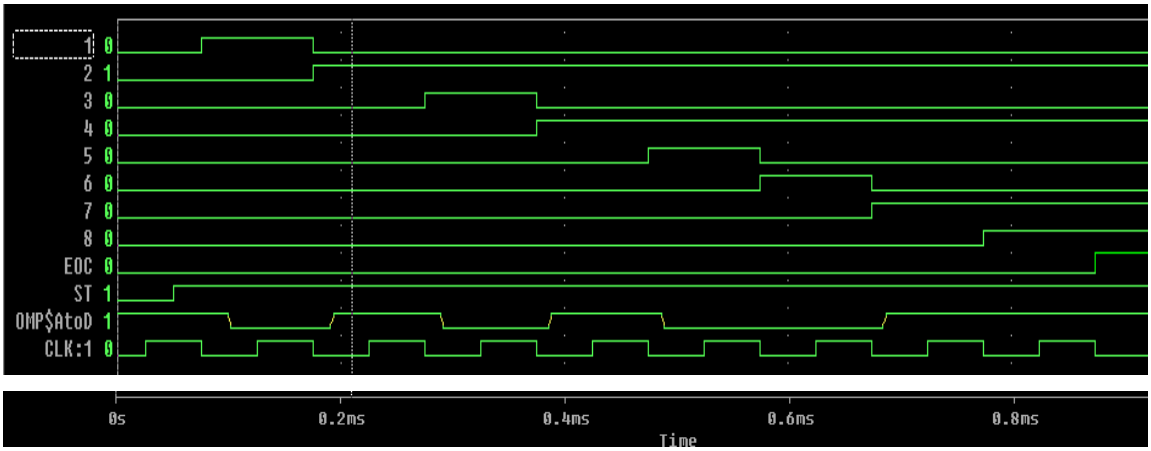


Figure 3.6: The EOC signal is sent directly after checking the LSB. This process lasted 9 CLK cycles where each cycle lasted 0.1ms.

After each EOC the circuit stays as it is waiting for the next START signal.

The conversion time depends mainly on the number of bits in the digital output to be produced that is N+1 clock cycles where N is the number of bits. The duration of the clock cycle is limited by the response time of some components in the circuit such as the FET transistors in the DAC circuit and the operational amplifiers used in the circuit.

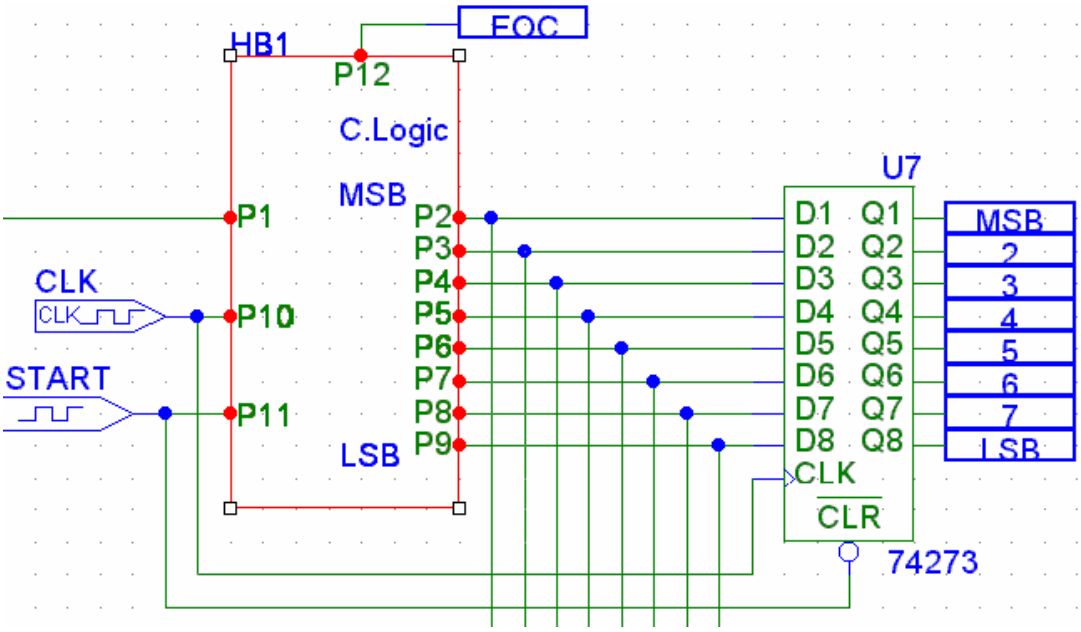


Figure 3.7: Part of the SAC circuit (Control Logic and the register).

Figure 3.7 in the previous page shows an 8-bit parallel-to-parallel register, which could be connected directly to the control logic outputs.