## 4.0 Introduction

This chapter provides general information about digital to analog information. It gives detailed information about Successive Approximation DAC. It also consists of the designing and testing process of the SAC.

## 4.1 General information

Digital to analog converter is a device used to convert the binary output of the digital processing system to a proportional analogue voltage or current. It takes a value in a digital code representation (Binary or BCD) and converts it to an analog voltage or current proportional to the digital code value.

The more the number of bits the digital to analog have, the smaller the step size and the finer the resolution is. Resolution is defined as the smallest change that can occur in the analog output as a result in the change of the digital input. It is –in other word- equal to the weight of the least significant bit (LSB). It is calculated from the equation below:

$$\textbf{Resolution} = \frac{Vref}{MSB}$$

where:
Vref is the reference voltage.
MSB is the weight of the most significant bit.

The output of the digital to analog converter is equal to the value of the reference voltage (Vref) multiplied by the value of the binary input (B) that ranges from 00000000 (0) to 11111111 (256) for an 8 bits digital to analog converter divided by the weight of the most significant bit (MSB) which is 128 in this case.

$$\textbf{Vout} = \frac{Vref}{MSB} \bullet \textbf{B}$$

The digital to analog plays a vital role in the analog to digital converter. It is used to convert the digital signal that comes from the control logic to a digital output signal that goes to the comparator as shown in figure 4.0

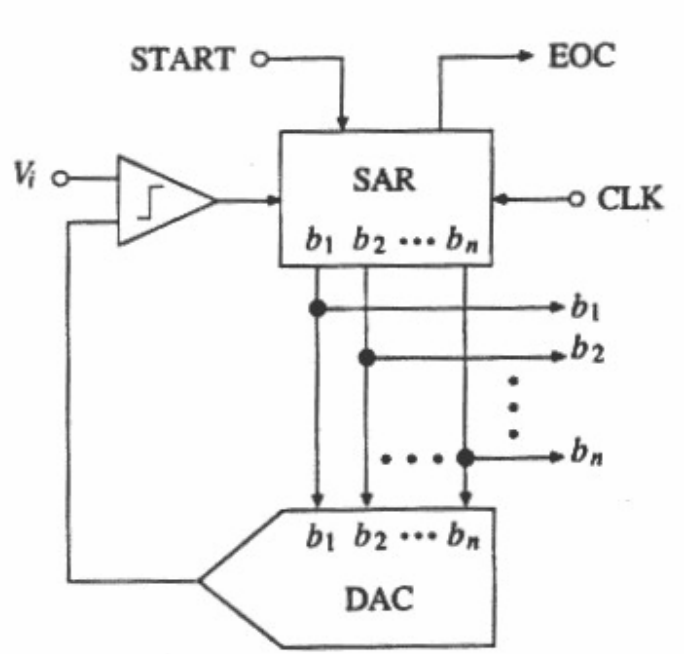


*Figure 4.0 SAC block diagram*

## 4.2 Types of DACs

There are mainly two typed of digital to analog converters mentioned below:

### 4.2.1 Binary weighted input digital to analog converter

In this method, a resistors network is used with resistor values that represent the binary weights of the input resistors, which might have current. When the digital input voltage is **high,** the amount of current will be depending on the input resistors, which have different values for each. On the other hand, when the digital input voltage is **low,** the current will be zero.

Figure 4.1 shown below shows a 4-bit binary weighted input digital to analog converter.

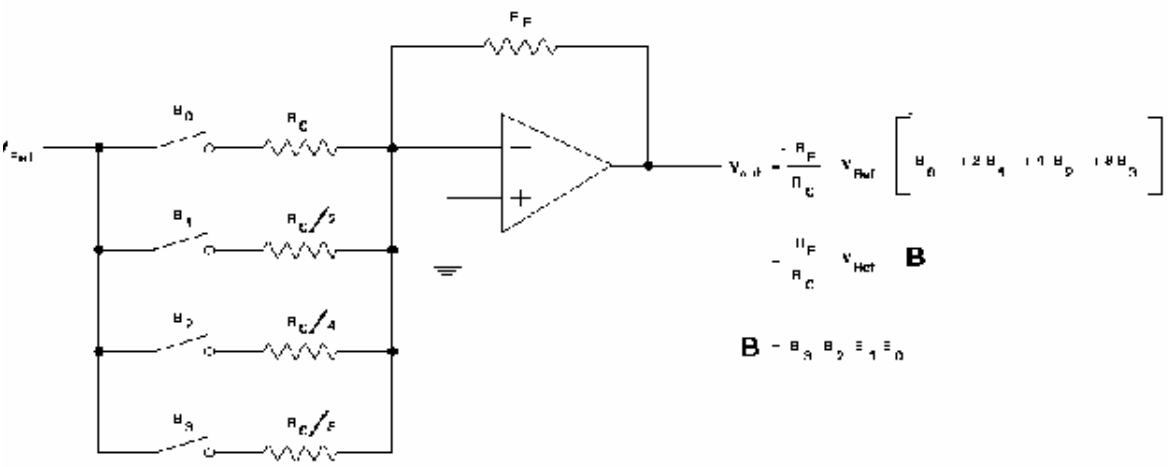

*Figure 4.1 4-bit binary-weighted DAC*

After that, all of the input currents will be summed and go through $R^F$ and since the inverting input is virtually grounded (0 V), so the output voltage will be equal to the voltage across $R^F$.

The values of the input resistors are chosen to be inversely proportional to the digital input binary weights. The output voltage is proportional to the sum of the input binary weights as shown in figure 4.1 above.

This binary weighted input digital to analog converter is not widely used because of its disadvantages. One of the disadvantages is the different value of resistors this binary weighted input digital to analog uses. That means; for eight bits digital to analog converter, eight resistor values will be needed, R and 8 multiples of it (i.e. R, 2R, 4R, 8R, …., 128 R or R, $\frac{R}{2}$, $\frac{R}{4}$,…., $\frac{R}{128}$)

### 4.2.2 R/2R ladder network digital to analog converter

This method of overcomes the disadvantage of the binary weighted input digital to analog converter by using only two standard resistor values. A 4-bit R/2R ladder digital to analog converter circuit is shown in figure 4.2 in the next page

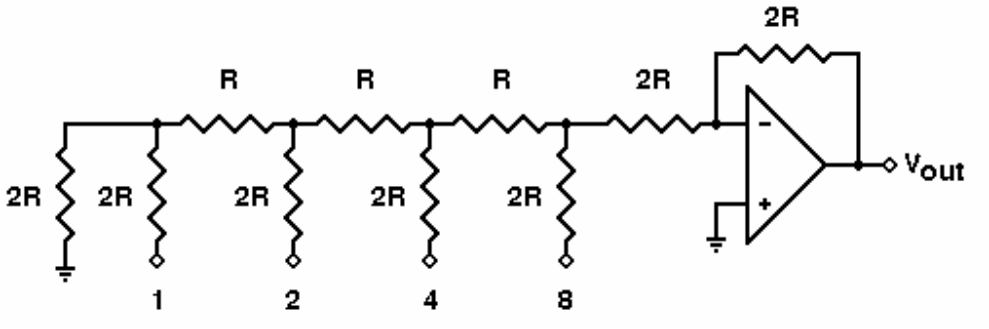


*Figure4.2 4-bit R/2R ladder network DAC*

The operational amplifier is a linear amplifier that has two inputs (inverting ands non-inverting) and one output. It has a very high voltage gain and very high input impedance. When it is used as an inverting amplifier, shown in figure4.3 below

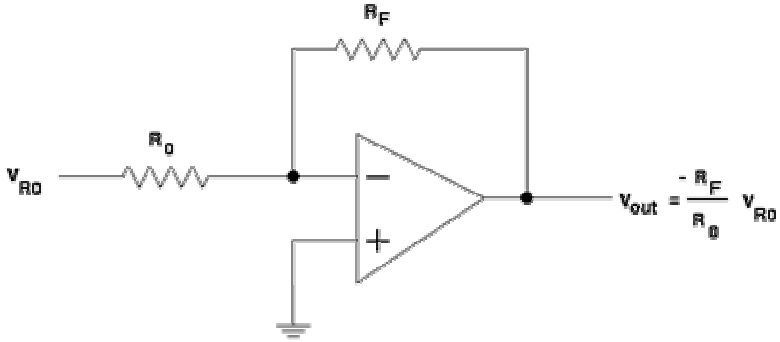


*Figure4.3 An inverting amplifier*

The feedback resistor and the input resistor, control the voltage gain according to the formula:

$$\frac{Vout}{Vin} = - \frac{Rf}{Ri}$$

In the inverting amplifier configuration, the inverting input of the operational amplifier is grounded as it is seen from figure 4.3 above.

## 4.3 The design and testing process:

At the beginning of the Successive approximation converter, a 2-bit converter was designed with two values of resistors R and 2R. The value of the resistors was chosen to be 200KΩ and 400KΩ as shown in figure 4.4 below shows the designed converter

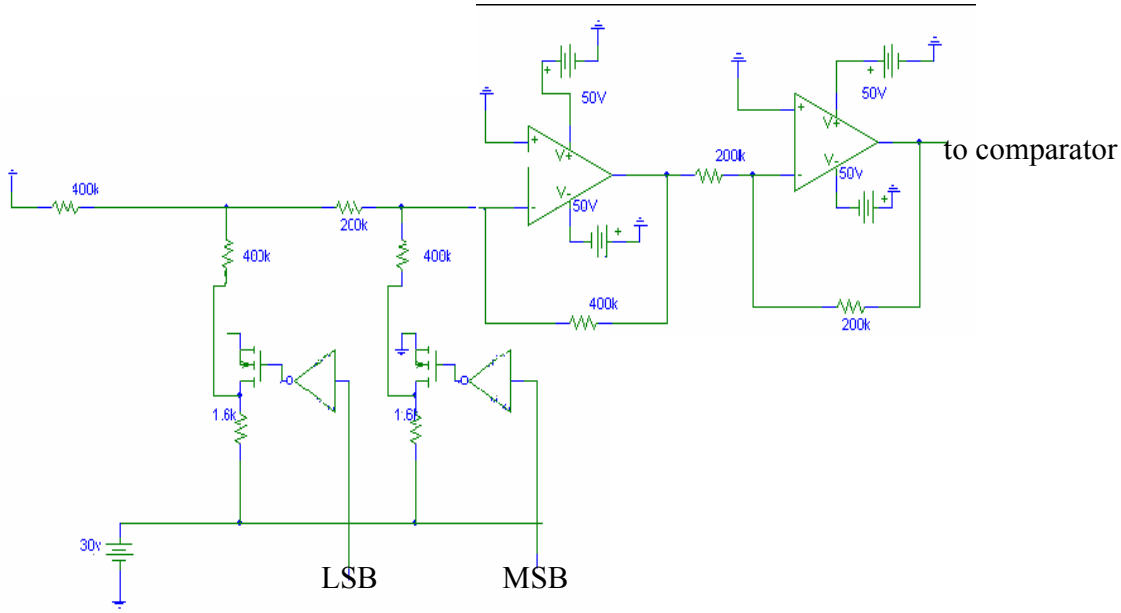


*Figure 4.4: 2-bit Successive approximation converter circuit*

After making sure that the designed converter is accurate by applying digital input voltages to the converter and measuring the resultant analog voltage, an 8-bit successive approximation digital to analog converter was designed. The designed 8-bit successive approximation converter circuit is shown in figure 4.5 in the next page.

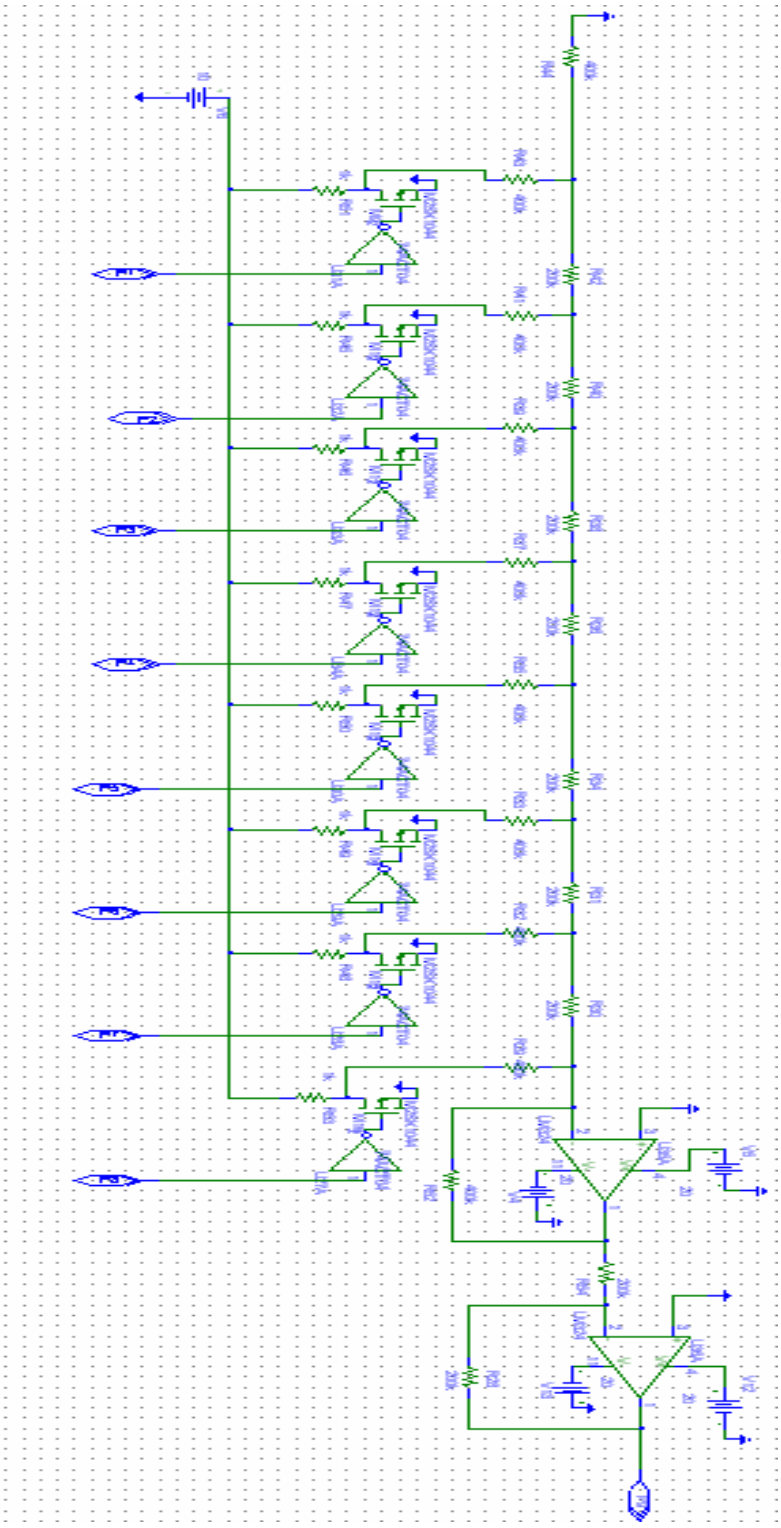

*Figure4.5: An 8-bit Successive Approximation DAC*

In order to make the process automatically switching, NMOS switches were used. NMOS switches that switch off (open circuit) when the digital voltage (bit) coming from the control logic is low (0) and switch on (short circuit) when the digital voltage (bit) coming from the control logic is high (1).

For testing, numbers of test input voltages were applied to the digital to analog converter. One of the testing voltages with circle around the output voltage is shown in figure 4.6 below

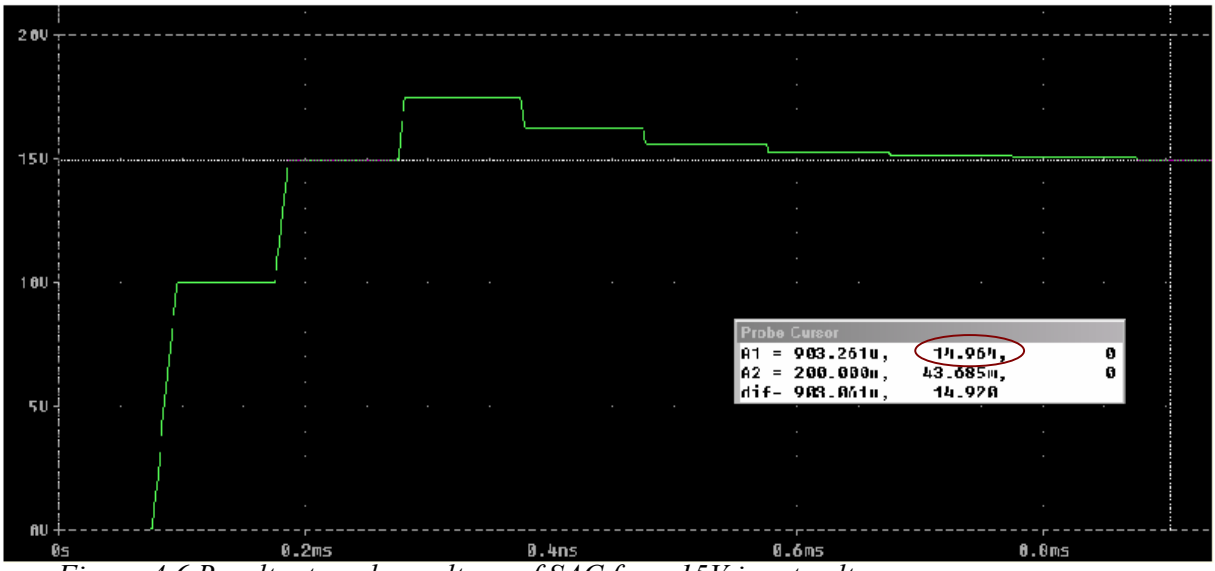


*Figure 4.6 Resultant analog voltage of SAC from 15V input voltage*

It is noticed in the previous example that the resultant analog voltage is 14.964V from a digital input voltage of 15V, which means a 0.036V error. It was found that it is an acceptable error for an 8-bit digital to analog converter by calculations shown below:

$$\textbf{Resolution} = \frac{Vref}{MSB} = \frac{10}{128} = 0.078125\text{V}$$

$$\textbf{Maximum acceptable error} = \frac{\text{Re}\,solution}{2} = 0.039063\text{V}$$

The error could be improved by, either increasing the number of bits or decreasing the reference voltage (Vref). If the second option is chosen, the characteristics of the NMOS

switches should be considered and the reference voltage (Vref) should be more than the required voltage to switch on those switches.

From figure 4.6 it is also noticed that the conversion time is 903.261u seconds (0.9m seconds) which is considered as a fast conversion time. This conversion time is fixed and will not be changed for all of the digital voltages values applied to the successive approximation digital to analog converter as it is mentioned previously in this chapter.